Serial No.: 09/620,474

REMARKS

As a preliminary matter, it is noted that the Examiner has not granted foreign priority on the assertion that the "application was filed more than twelve months" after the filing of the Japanese application. However, this assertion is based on an incorrect filing date of November 6, 2000 for the present application. The correct filing date is July 20, 2000. It appears the PTO has improperly changed the filing date based on Applicants' filing of a "Response to Notice of Missing Parts of Application" on November 6, 2000. A Request for Corrected Filing Receipt to change the filing date of the present application in PTO records is being filed under separate cover.

The indication of allowable subject matter in claims 14-16 is acknowledged and appreciated. In view of the following remarks, it is respectfully submitted that all claims are in condition for allowance.

Claims 7, 9, 12, 17 and 20 are independent and stand rejected under 35 U.S.C. § 103 as being unpatentable over Mahmud 1 in view of Amadori. This rejection is respectfully traversed for the following reasons.

Each of independent claims 7, 9, 12, 17 and 20 embody a method of designing an interface using plural libraries corresponding to plural ***applications***. Accordingly, in order to analyze an interface, the present invention can simulate ***actual*** operation of a semiconductor integrated circuit. In contrast, Mahmud 1 is a technical paper directed merely to ***theoretical*** simulation. That is, Mahmud 1 does not disclose libraries for applications. Mahmud 1 uses only the ***possibility*** of a request for bus access, whereas the present invention can simulate actual operation of, for example, an LSI using libraries corresponding to operation models of plural applications. As summarized in Table 1 on

page 124, Mahmud 1 merely describes analytical results which are mathematically-based and computer-generated simulation results which are probability-based, as opposed to actual results which are based on real operation as can be performed in the present invention. Mahmud 1 is completely unrelated to, and does not enable, a real operational model in which operations are actually simulated using ***libraries***. Indeed, as noted on page 125, col. 2, lines 6-7, Mahmud 1 expressly states that "[t]his paper presents the ***preliminary*** model" (emphasis added) of a bus system.

In view of the deficiencies of Mahmud 1, the Examiner relies on Amadori as disclosing VHDL component models for bus components. However, it is respectfully submitted that Amadori does not overcome the deficiencies of Mahmud 1. VHDL is merely a conventional modeling language used to design ***architecture*** rather than ***applications***.

In order to expedite prosecution, a personal interview was conducted with Examiners Sharon and Ferris. Applicant and Applicant's representative would like to thank Examiner Sharon and Ferris for their courtesy in conducting the interview and for their assistance in resolving issues. During the interview, the Examiners requested that Applicant clarify the distinction between an "application" as used in the present invention and conventional architecture design.

Generally speaking, an "application" is a particular job which is executed by software, hardware, or a combination thereof. In this regard, an aspect of the present invention includes designing a kind of architecture of the processor ***according to an application(s)*** which is executed by the processor. Examples of an "application" include a transfer operation of print data by using IrDA, a transfer of the positional data of a

mouse by using USB, and compression and decompression of still image data by using JPEG, etc. (*see, e.g.,* page 17, lines 22-25 of Applicant's specification). An "application" can be divided into plural functions (i.e., "layers"). For example, "FLOW", "MANG", and "LINK" are functions which are parts of an "application" (*see, e.g.*, Fig. 6 of Applicant's drawings and corresponding text). In contrast, "architecture" is merely the structure of hardware. For example, the bus structure and memory configuration are parts of architecture.

During the interview, Examiner Sharon raised the possible relevance of prior art (as of yet un-cited) related to large scale network design to processor design. The following remarks address this issue. As an intended use of the present invention, in a processor, for example, a bus connects plural components (where each component has a specific function) that can be inter-dependent so as to do a particular job (i.e., application). A few examples of such components include a memory, CPU and an A/D converter. In contrast, a network connects "terminals" where each "terminal" does not have a specific function and is operationally independent of other terminals. An example of a "terminal" used in a large scale network is a personal computer.

Turning to the distinctions between an "application" of the present invention and the architecture disclosed by Amadori, exemplary operation models of the present invention are described in Fig. 6 of Applicant's drawings (i.e., APPLI_A 100, APPLI_B 80, and APPLI_C 80). The result of an exemplary simulation where operation models are applied to specific architecture is described in Fig. 7 of Applicant's drawings (e.g., actual application is operated in the time sequence using the operation model described in

Fig. 7). In contrast, as discussed above, VHDL as disclosed by Amadori is merely modeling language which describes architecture (e.g., memory, bus).

As is well known, VHDL stands for VHSIC Hardware Description Language. Using VHDL, hardware components such as a Memory and Bus are described as description models. Amadori discloses only a method of designing using such VHDL. But VHDL itself is not related to an "application" as described above, whereas the present invention can simulate actual operation of an application (*see, e.g.*, page 17, lines 22-25 of Applicant's specification). Indeed, Amadori does not disclose simulation of an application, let alone simulation for actual operation of an application.

Accordingly, even assuming *arguendo* proper, the proposed combination does not disclose or suggest the claimed invention. The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claims 7, 9, 12, 17 and 20 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Moreover, it is respectfully submitted that the proposed combination is improper as lacking proper motivation. It is emphasized that only Applicant has conceived and enabled the novel and non-obvious ***combination*** of using libraries containing applications for interface design. Accordingly, even assuming *arguendo* that Amadori disclosed application-containing libraries, the cited prior art nonetheless would not suggest using

such application-containing libraries in actual operation simulations for interface design. Rather, at best, the cited prior art would still only suggest theoretical simulation of the applications. In such a hypothetical, the cited prior art would fail to evidence a *prima facie* showing of obviousness that the ***combination*** of elements recited in the claims is known or suggested in the art. For the foregoing reasons, it is submitted that the proposed combination of Mahmud 1 and Amadori is improper.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 7, 9, 12, 17 and 20 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on all the foregoing, it is submitted that claims 7-27 are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 102/103 be withdrawn.

CONCLUSION

Having fully and completely responded to the Office Action, Applicant submits that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an

interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: March 29, 2004